MIFARE ULTRALIGHT User Manual

Release 1.0.0

SonMicro Elektronik

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CHAPTER

ONE

INTRODUCTION

Note: This document focuses quick understanding of the MIFARE® Ultralight EV1 (and MIFARE® Ultralight) cards and their usage. For more information about the MIFARE® Ultralight EV1 family of tags please refer NXP Semiconductor datasheets.

The MIFARE® CLASSIC family, including the MIFARE® Ultralight, is the most widely used contactless smart card ICs operating in the 13.56 MHz frequency range with read/write capability and ISO/IEC 14443 A compliance. Smart cards based on MIFARE® are a commonly known solution in various applications such as:

- Access Control
- Public Transportation
- Electronic Toll Collection
- Loyalty Cards
- Event Ticketing
- Car Parking
- and many more...

MIFARE Ultralight family of tags is being used in short range (up to 10 centimeters - depends on tag and antenna size) RFID applications include single trip or limited use tickets in public transportation networks, loyalty cards or day passes for events. It serves as a replacement for conventional ticketing solutions such as paper tickets, magnetic stripe tickets or coins. It is also a perfect ticketing counterpart to contactless card families such as MIFARE® DESFire or MIFARE® Plus. It also supports anti-collision feature so that multiple cards in the field can work.

- **MIFARE® Ultralight EV1(MF0 ULx1)**
  - 7-byte UID (serial number)
  - 384 and 1024 Bits user memory product variant (20 pages a 4-byte, 41 pages a 4-byte)
  - 32-bit OTP (One Time Programmable) area
  - Lock bits, Configurable Counters
  - Three independent 24-bit one-way counters (comes with EV1)
  - Protected data access through 32-bit password (comes with EV1)
  - Anti-collision support
  - Memory overwrite protection
  - Write Endurance: 100 000 Cycle, 10 years data retention
  - Write Endurance for one-way counters 1.000.000 cycles

MIFARE Ultralight differs from MIFARE Classic family (Mifare 1K/4K). The contactless communication is not encrypted. However, it is perfectly designed for **single or limited-use tickets** in public transport, event ticketing (i.e. stadiums, exhibitions, leisure parks etc.) and loyalty applications.

The MIFARE Ultralight EV1 is succeeding the MIFARE Ultralight ticketing IC and is fully functional backwards compatible. Its enhanced feature and command set enable more efficient implementations and offer more flexibility in system designs.

Note: MIFARE Ultralight EV1 is back-compatible with the Mifare Ultralight. However additional features that comes with EV1 (password access and Read/Increment counters) is not supported in **stdMifare V2.0.x** and previous firmware versions. Please ask for the availability of latest firmware version supporting the MIFARE Ultralight EV1 features. stdMifare V2.0.x and the previous versions fully supports MIFARE Ultralight (not the EV1)

CHAPTER

TWO

MIFARE ULTRALIGHT MEMORY ORGANIZATION

2.1 MIFARE ULTRALIGHT MEMORY MAP

	Byte Number within Page				
Page	0	1	2	3	**Description**
0	UID0	UID1	UID2	CB0	Serial Number Part1 + Check Byte0
1	UID3	UID4	UID5	UID6	Serial Number Part2
2	CB1	Int.	LCK0	LCK1	Check Byte1 and Lock Configuration
3					OTP (One Time Programmable) Area
4					Data Page
5					Data Page
6					Data Page
7					Data Page
8					Data Page
9					Data Page
10					Data Page
11					Data Page
12					Data Page
13					Data Page
14					Data Page
15					Data Page
MIFARE Ultralight Ev1 is compatible with Mifare Ultralight but has additional features and pages as below:					
16	CFG0				Configuration Page
17	CFG1				Configuration Page
18	PWD				Configuration Page
19	PACK		RFU		Configuration Page
	One way counters				Counter pages

Table 2.1 *MIFARE Ultralight/EV1 - Memory Organization*

- MIFARE Ultralight consist of 16 pages, each page has 4 bytes.
- MIFARE Ultralight has 384-bit user read/write area (12 pages).
- MIFARE Ultralight EV1 consist of 20 pages, each page has 4 bytes.
- MIFARE Ultralight EV1 has 384-bit user read/write area (12 pages). 1024-bit user r/w area(32 pages) available.
- Page0 and Page1 hold unique Serial Number (Read-Only)
- Page2 holds lock configuration of pages
- Page3 is a special One Time Programmable area. Once any bit of Page2 (Lock) and Page3 (OTP) is set to “1” it will never be possible to program that bit as “0”.

- MIFARE Ultralight EV1 comes with new features such as password access and one-way counters.

CHAPTER

THREE

MIFARE ULTRALIGHT PAGES

Mifare Ultralight memory can be categorized into following types:

- Manufacturer Data and Lock Configuration
- One-Time-Programmable (OTP) Area
- User Data Pages
- Configuration Pages (comes with EV1)
- Counter Pages (One-way Counters, comes with EV1)

3.1 MANUFACTURER DATA & LOCK CONFIGURATION

3.1.1 UID/Serial Number

The unique 7-byte serial number (UID) and its two check bytes are programmed into the first 9 bytes of memory covering page addresses 00h, 01h and the first byte of page 02h. The second byte of page address 02h is reserved for internal data. These bytes are programmed and write protected in the production test.

Remark: Generally the UID is retrieved at card activation sequence instead of reading these pages directly.

Note:

- CB0 = 0x88 **xor** UID0 **xor** UID1 **xor** UID2
- CB1 = UID3 **xor** UID4 **xor** UID5 **xor** UID6
- SN0 holds the Manufacturer ID for NXP Semiconductors (04h) in accordance with ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1

3.1.2 LOCK CONFIGURATION

- Byte2(LCK0) and Byte3(LCK1) of page 02h represent the field programmable read-only locking mechanism.
- Each page from 03h (OTP) to 0Fh can be individually locked by setting the corresponding locking bit Lx to logic 1 to prevent further write access. After locking, the corresponding page becomes read-only memory **permanently**

Attention: Lock operation is irreversible. When a bit is set in lock configuration, it cannot be changed back to logic 0.

LCK0 - Lock Byte 0 (Byte2 of Page2)							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
L7	L6	L5	L4	L OTP	BL 15-10	BL 9-4	BL OTP

Table 3.1.2 *Lock Byte0*

bit0 - BL OTP (Block Lock OTP)

- 0: Do not freeze lock config for OTP
- 1: Freeze lock config for OTP. bit3 - L OTP cannot be used again.

bit1 - BL 9-4 (Block Lock Config for Pages 4 to 9)

- 0: Do not freeze lock config for Page[4-9]
- 1: Freeze lock config for Page[4-9]. L4,L5,L6,L7,L8,L9 bits cannot be used again.

bit2 - BL 15-10 (Block Lock Config for Pages 10 to 15)

- 0: Do not freeze lock config for Page[10-15]
- 1: Freeze lock config for Page[10-15]. L10,L11,L12,L13,L14,L15 bits cannot be used again.

bit3 - L OTP (Lock OTP Page)

- 0: Do not lock OTP Page
- 1: Locks OTP Page (makes it read-only permanently)

bit4 - L4 (Lock Page4)

- 0: Do not lock Page4
- 1: Locks Page4 (makes it read-only permanently)

bit5 - L5 (Lock Page5)

- 0: Do not lock Page5
- 1: Locks Page5 (makes it read-only permanently)

bit6 - L6 (Lock Page6)

- 0: Do not lock Page6
- 1: Locks Page6 (makes it read-only permanently)

bit7 - L7 (Lock Page7)

- 0: Do not lock Page7
- 1: Locks Page7 (makes it read-only permanently)

LCK1 - Lock Byte 1 (Byte3 of Page2)							
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
L15	L14	L13	L12	L11	L10	L9	L8

Table 3.1.2 *Lock Byte1*

bit0 - L8 (Lock Page8)

- 0: Do not lock Page8
- 1: Locks Page8 (makes it read-only permanently)

bit1 - L9 (Lock Page9)

- 0: Do not lock Page9
- 1: Locks Page9 (makes it read-only permanently)

bit2 - L10 (Lock Page10)

- 0: Do not lock Page10
- 1: Locks Page10 (makes it read-only permanently)

bit3 - L11 (Lock Page11)

- 0: Do not lock Page11
- 1: Locks Page11 (makes it read-only permanently)

bit4 - L12 (Lock Page12)

- 0: Do not lock Page12
- 1: Locks Page12 (makes it read-only permanently)

bit5 - L13 (Lock Page13)

- 0: Do not lock Page13
- 1: Locks Page13 (makes it read-only permanently)

bit6 - L14 (Lock Page14)

- 0: Do not lock Page14
- 1: Locks Page14 (makes it read-only permanently)

bit7 - L15 (Lock Page15)

- 0: Do not lock Page15
- 1: Locks Page15 (makes it read-only permanently)

3.2 OTP AREA

Page 03h is the OTP page and it is preset so that all bits are set to logic 0 after production. These bytes can be bit-wise modified using the CmdWriteBlock4Byte command. (See relevant application Firmware Manual, e.g. stdMifareV2.x.x)

The parameters of the write command (the value to be written) is bit-wise OR'ed with the current contents of the OTP bytes. The result is the new OTP byte contents. This process is irreversible and once a bit is set to logic 1, it cannot be changed back to logic 0.

The default value of the OTP bytes is 00 00 00 00h.

This memory area can be used as a 32 tick one-time counter.

Remark: Any write operation to the OTP bytes features anti-tearing support.

Anti-tearing mechanism provides the verification of data integrity and data consistency when the card is pulled out of the RF field or if the card has not enough power to complete a certain operation.

3.3 USER DATA PAGES

Pages 04h to 0Fh for the MF0UL11 and 04h to 23h for the MF0UL21 are the user memory read/write area. The access to a part of the user memory area can be restricted using a password verification (password access feature comes with EV1).

Remark: The default content of the data blocks at delivery is not defined

3.4 CONFIGURATION PAGES

Configuration pages comes with MIFARE Ultralight **EV1**. Supporting firmware for EV1 features is available upon request. This section is intended to be completed after public release of supporting firmware.

For more details on Configuration Pages, please check section 8.5.6 on MF0ULx1(MIFARE Ultralight EV1 - Contactless ticket IC) datasheet that can be accessed at NXP Semiconductor website.

3.5 COUNTER PAGES

Counter pages comes with MIFARE Ultralight **EV1**. Supporting firmware for EV1 features is available upon request. This section is intended to be completed after public release of supporting firmware.

For more details on One-Way-Counters Pages, please check section 8.7 on MF0ULx1(MIFARE Ultralight EV1 - Contactless ticket IC) datasheet that can be accessed at NXP Semiconductor website.

CHAPTER

FOUR

TRADEMARKS

- MIFARE® is a registered trademark of NXP B.V. and is used under license.
- NTAG® is a trademark of NXP B.V

CHAPTER

FIVE

DOCUMENT REVISON HISTORY

Version 1.0.0 (22 Oct 2017)

Initial release.